PRODUCT BRIEF

Kintex UltraScale+ FPGAs

BEST PRICE/PERFORMANCE/WATT FOR THE MID-RANGE

Kintex® UltraScale+™ FPGAs deliver the industry's most cost-effective solution for system performance-per-watt with ASIC-class serial connectivity. These devices expand the mid-range by delivering the highest throughput with lowest latency for medium-to-high volume applications that include wireless MIMO, NX100G networking, and DSP-intensive applications. Based on the ASIC-class advantage of the UltraScale™ architecture, Kintex UltraScale+ devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

RE-ARCHITECTING THE CORE FOR MASSIVE BANDWIDTH WITH THE ULTRASCALE ARCHITECTURE

The UltraScale+ families are based on the first all programmable architecture to span multiple nodes from planar through FinFET technologies, and from monolithic through 3D ICs. Xilinx UltraScale architecture provides diverse benefits and advantages to an array of markets and applications. The architecture combines enhancements in the configurable logic blocks (CLB), a dramatic increase in device routing, and a revolutionary ASIC-like clocking architecture, with high-performance DSP, memory interface PHYs, and serial transceivers. All UltraScale architecture-based FPGAs are capable of pushing the system performance-per-watt envelope enabling breakthrough speeds with high utilization. High system performance and multiple power reduction innovations make the UltraScale architecture the logical choice for many next-generation applications.

BUILDING ON THE SUCCESS OF XILINX'S ULTRASCALE PORTFOLIO

The UltraScale+ family of FPGAs, 3D ICs, and MPSoCs, combines UltraRAM, 3D-on-3D, and MPSoC technologies, delivering an extra node of value. To enable an even higher level of performance and integration, the UltraScale+ family also includes the IP interconnect optimization technology, SmartConnect. Built upon Xilinx's UltraScale architecture, they leverage a significant boost in performance-per-watt using 16FF+ FinFET 3D transistors from the #1 service foundry in the world, TSMC. Xilinx provides scalability and package migration for the lowest risk and the highest value programmable technology.

TARGET APPLICATIONS

DATA CENTER

- Network Acceleration
- Storage Acceleration

INDUSTRIAL, SCIENCE, AND MEDICAL

- Medical Imaging
- Machine Vision

WIRED COMMUNICATIONS

- PON Access
- Optical Transport Network (OTN)

WIRELESS COMMUNICATIONS

- Radio
- Baseband

FEATURES OVERVIEW

16nm low power FinFET+ process technology from TSMC Industry-leading process from the #1 service foundry delivers a step function increase in performance-per-watt	• Over 2X performance-per-watt over Kintex-7 FPGAs • The same scalable architecture and tools from Kintex UltraScale FPGAs
UltraRAM for deep memory buffering Up to 36Mb for SRAM device integration	• For deep packet and video buffering • 8X capacity-per-block vs. traditional embedded memory • Deep-sleep power modes
SmartConnect technology System-wide interconnect optimization tools and IP	• Matches optimal AXI interconnect to the design • Automatic interface bridging • Additional 20–30% advantage in performance-per-watt
Massive I/O bandwidth and dramatic latency reduction 50% greater serial bandwidth than Kintex UltraScale devices, and 4X greater than Kintex-7 devices	• 16G and 28G backplane support • 32.75G chip-to-chip and chip-to-optics support • High-Density I/O for greater area and power efficiency per pin
Enhanced routing, ASIC-class clocking, and efficient fabric Enabling breakthrough speeds with high utilization	• Smaller area and greater power consistency • Up to two speed-grade advantage vs. comparable solutions • Efficient CLB use and placement for reduced interconnect delay
Massive memory interface bandwidth Next-generation DDR and serial memory support	• DDR4 support of up to 2,666Mb/s • Support for server-class DIMMs (8X capacity vs. Kintex-7) • Hybrid Memory Cube serial memory support of up to 30G
Integrated blocks for PCI Express® Complete end-to-end solution for multi-100G ports	• Gen3 x16 and Gen4 x8 for 100G bandwidth per block • Expanded virtualization for data center applications • Enhanced tag management for increased buffer space
Integrated 100G Ethernet MAC and 150G Interlaken cores ASIC-class cores for breakthrough performance in packet processing	• 60K—100K system logic cell savings per port • Up to 90% dynamic power savings vs. soft implementation • Built-in KR4 RS-FEC (Ethernet MAC) for optics error correction
Enhanced DSP slices for diverse applications Enabling a massive jump in fixed- and floating-point performance	• Up to 6.3TeraMACs of bandwidth at 891MHz operation • Double-precision floating point using 30% fewer resources • Complex fixed-point arithmetic in half the resources
High-speed memory cascading Removes key bottlenecks in DSP and packet processing	• Eliminates fabric usage when building deep memories • Reduces routing congestion • Lowers dynamic power consumption
Up to 50% power savings over Kintex-7 devices, and 30% power saving over Kintex UltraScale devices Static- and dynamic-power optimizations at every level	• Optimal voltage tuning • Power-optimized transceivers and block RAM • More granular clock gating of logic fabric and block RAM
Security Enhanced features to protect IP and prevent tampering	• AES-GCM decryption, RSA-2048 authentication • DPA countermeasures and permanent tamper penalty • Improved SEU performance

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